(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平11－317451

(43)公開日　平成11年(1999)11月16日

(51)Int.Cl.[6]		識別記号	FI		
Ｈ０１Ｌ	21/768		Ｈ０１Ｌ	21/90	Ｖ
	21/28	３０１		21/28	３０１Ｒ
	21/3205			21/88	Ｍ

審査請求　未請求　請求項の数15　ＯＬ　（全 21 頁）

(21)出願番号　特願平10－124816

(22)出願日　平成10年(1998)５月７日

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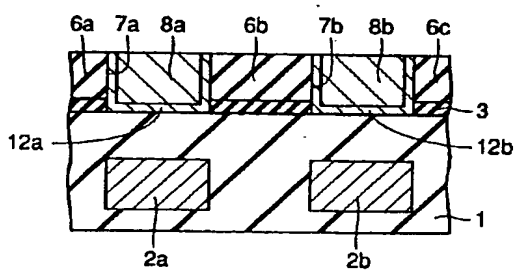
(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】

【課題】　配線間の容量の増大を防止し、動作速度の低下を防止することが可能な半導体装置およびその製造方法を提供する。

【解決手段】　導電領域２ａ、２ｂと第１の絶縁膜１と被覆膜３と第２の絶縁膜６ａ～６ｃと配線層８ａ、８ｂとを備える半導体装置において、第１の絶縁膜１は導電領域２ａ、２ｂ上に形成されている。被覆膜３は第１の絶縁膜１の表面を露出させる貫通孔を有し、第１の絶縁膜１上に形成されている。第２の絶縁膜６ａ～ｃは、貫通孔上に形成され、第１の絶縁膜１の表面を露出させる溝７ａ、７ｂを有する。溝７ａ、７ｂの内部に配線層８ａ、８ｂが形成されている。



English Translation of JP 11-317451A

(2)

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

[Claim(s)]

[Claim 1] The thickness of the aforementioned covering film [in / the 1st field of the above / it has the 2nd insulator layer and the wiring layer formed in the interior of the aforementioned slot characterized by providing the following, and] is a semiconductor device thinner than the thickness of the aforementioned covering film in the 2nd field of the above. Electric conduction field. The 1st insulator layer formed on the aforementioned electric conduction field. The covering film which is formed on the insulator layer of the above 1st and has the 1st field and 2nd field. It is formed on the aforementioned covering film and is a slot on the field of the above 1st.

[Claim 2] The semiconductor device characterized by providing the following. Electric conduction field. The 1st insulator layer formed on the aforementioned electric conduction field. The covering film which has the breakthrough to which it is formed on the insulator layer of the above 1st, and the front face of the 1st insulator layer of the above is exposed. The wiring layer which was formed on the aforementioned breakthrough and formed in the 2nd insulator layer which has the slot into which the front face of the 1st insulator layer of the above is exposed, and the interior of the aforementioned slot.

[Claim 3] The semiconductor device according to claim 1 or 2 characterized by providing the following. The aforementioned slot is the 1st slot. The field located between the above 1st and the 2nd slot is a field in which the aforementioned covering film is not formed including the 1st wiring layer and the 2nd wiring layer by which the aforementioned wiring layer was formed in the interior of the 1st slot of the above, and the 2nd slot of the above, respectively including the 2nd slot formed by separating the 1st slot of the above, and distance.

[Claim 4] A semiconductor device equipped with the 1st and 2nd wiring layers formed, respectively on an insulator layer, the 1st covering film formed on the aforementioned insulator layer, the 2nd covering film formed by separating the covering film and interval of the above 1st on the aforementioned insulator layer, and the above 1st and the 2nd covering film.

[Claim 5] the field which is further equipped with the conductor film which connects electrically the electric-conduction field formed in the bottom of the aforementioned insulator layer, and the wiring layer and the aforementioned electric-conduction field of the above 1st, and is located under the wiring layer of the above 1st -- setting -- the covering film and the aforementioned insulator layer of the above 1st -- connection -- a hole forms -- having -- the aforementioned connection -- the semiconductor device

according to claim 4 with which the aforementioned conductor film is formed in the interior of a hole

[Claim 6] It is the semiconductor device according to claim 4 or 5 with which it has further the up insulator layer formed on the above 1st and the 2nd covering film, the 1st and 2nd slots are formed in the field located on the above 1st and the 2nd covering film at the aforementioned up insulator layer, respectively, and the above 1st and the 2nd wiring layer are formed in the interior of the above 1st and the 2nd slot, respectively.

[Claim 7] The aforementioned covering film is a silicon nitride, a silicon oxidization nitride, the silicon nitride containing a fluorine, a silicon oxidization nitride containing a fluorine, and aluminum 2O3. aluminum 2O3 containing a film and a fluorine Semiconductor device given in any 1 term containing at least one chosen from the group which consists of a film of claims 1-6.

[Claim 8] claim 1- containing at least one chosen from the group which the aforementioned wiring layer and an electric conduction field become from Cu, Cu alloy, aluminum, aluminum alloy, Ag, Ag alloy, Au, W, WN and TiN, TiWN, Ta and TaN, and a doped polysilicon -- a semiconductor device given in any 1 term of 3 and 5

[Claim 9] A semiconductor device given in any 1 term of claims 1-8 by which the barrier metal layer is formed in the front face of the aforementioned wiring layer.

[Claim 10] The aforementioned barrier metal layer is a semiconductor device containing at least one chosen from the group which consists of a nitride of the alloy containing the nitride of a refractory metal and a refractory metal, the nitride of a refractory metal and silicon, and two or more kinds of refractory metals, and the alloy containing two or more kinds of refractory metals according to claim 9.

[Claim 11] The process which forms the electric-conduction field characterized by to provide the following, the process which form the 1st insulator layer on the aforementioned electric-conduction field, the process which form a covering film on the insulator layer of the above 1st, the process which form the 2nd insulator layer on the aforementioned covering film, the process which form the slot which exposes the front face of the aforementioned covering film to the 2nd insulator layer of the above by etching, and the bottom of the aforementioned slot. The process which removes some aforementioned covering films by etching. The process which forms a wiring layer in the interior of the aforementioned slot.

[Claim 12] The process which forms the electric-conduction field characterized by to provide the following, the process which form the 1st insulator layer on the aforementioned electric-conduction field, the process which form a covering film on the insulator layer of the above 1st, the process which form the 2nd insulator layer on the

aforementioned covering film, the process which form the slot which exposes the front face of the aforementioned covering film to the 2nd insulator layer of the above by etching, and the bottom of the aforementioned slot. The process which removes the aforementioned covering film by etching so that the front face of the 1st insulator layer of the above may be exposed. The process which forms a wiring layer in the interior of the aforementioned slot.

[Claim 13] The manufacture method of a semiconductor device equipped with the process which forms an insulator layer, the process which forms the 1st covering film on the aforementioned insulator layer, the process which separates the covering film and interval of the above 1st and forms the 2nd covering film on the aforementioned insulator layer, and the process which forms the 1st and 2nd wiring layers on the above 1st and the 2nd covering film, respectively.

[Claim 14] By removing some of processes which form an electric conduction field in the field located under the wiring layer of the above 1st under the aforementioned insulator layer, and the aforementioned insulator layers and the covering films of the above 1st by etching the connection to which the front face of the aforementioned electric conduction field is exposed -- the process which forms a hole, and the aforementioned connection -- the manufacture method of a semiconductor device according to claim 13 further equipped with the process which forms in the interior of a hole the conductor film which connects electrically the aforementioned electric conduction field and the wiring layer of the above 1st

[Claim 15] The process which forms the above 1st and the 2nd wiring layer which are characterized by providing the following is the process which forms an up insulator layer on the above 1st and the 2nd covering film, and a field located on the above 1st and the 2nd covering film. The process which forms the 1st and 2nd slots in the aforementioned up insulator layer by etching. The process which forms an electric conduction field in the field located under the wiring layer of the above 1st under the aforementioned insulator layer including the process which embeds the above 1st and the 2nd wiring layer to the interior of the above 1st and the 2nd slot, respectively. The process which forms opening by removing some covering films of the above 1st by etching. The aforementioned opening.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] More specifically, this invention relates

to the semiconductor device which can reduce the capacity during wiring, and its manufacture method about a semiconductor device and its manufacture method.

[0002]

[Description of the Prior Art] To the wiring used in a semiconductor device, improvement in a dimensional accuracy, reservation of the flat nature in multilayer-interconnection structure, and a demand further called simplification of the process for process cost reduction are becoming still severer with high integration of semiconductor devices, such as LSI. Then, after processing wiring recently, the flush-type wiring process (it is called the DAMASHIN method below) proposed as a completely different concept from the conventional wiring formation method which deposits and carries out flattening of the layer insulation film attracts attention. By the DAMASHIN method, a slot is first formed in an insulator layer. Wiring is formed by embedding this slot by metal membranes, such as copper, and removing the metal membrane further formed in portions other than a slot by methods, such as the chemical machinery grinding method (it being called the CMP method below). Drawing 41 is a cross section for explaining the wiring formed by this DAMASHIN method. Hereafter, with reference to drawing 41 , the structure of the wiring formed by the conventional DAMASHIN method is explained.

[0003] With reference to drawing 41 , a slot 113 is formed in the layer insulation film 101 which consists of a silicon oxide etc. first with the wiring structure by the conventional DAMASHIN method. The barrier metal layer 112 which consists of TiN etc. is formed in the interior of this slot 113. The wiring 102 which consists of Cu etc. is formed on the barrier metal layer 112. In order to prevent diffusion of Cu which constitutes wiring 102 on wiring 102 and the layer insulation film 101, the covering film 105 which consists of a silicon oxide etc. is formed in it. The layer insulation film 104 is formed on the covering film 105.

[0004] By forming wiring using such a DAMASHIN method, high aspect processing of required aluminum becomes unnecessary in the process which forms wiring of conventional aluminum. moreover, insulator layer ****** of a high aspect ratio -- it becomes unnecessary Consequently, the merit that flattening can be easily performed in multilayer-interconnection structure is obtained.

[0005] Furthermore, in order to integrate a semiconductor device highly, it is required to multilayer-structure-ize wiring. And the example of the semiconductor device which has the multilayer-interconnection structure formed using the above DAMASHIN methods is shown in drawing 42 . With reference to drawing 42 , the semiconductor device which has the multilayer-interconnection structure using the DAMASHIN method is

explained.

[0006] With reference to drawing 42 , lower layer wiring and the becoming wiring 102a and 102b are formed on a semiconductor substrate (not shown). These wiring 102a and 102b may be formed by the DAMASHIN method as shown in drawing 41 , and may be formed by processing a conventional polysilicon contest film, a conventional aluminum film, etc. by etching etc. The layer insulation film 101 which consists of a silicon oxide etc. is formed on wiring 102a and 102b. The etching stopper layer 103 which consists of a silicon nitride etc. is formed on the layer insulation film 101. The layer insulation films 106a-106c are formed on the etching stopper layer 103. These layer insulation films 106a-106c have the slots 107a and 107b for forming Wiring 108a and 108b. The wiring 108a and 108b which consists of Cu etc. is formed in the interior of Slots 107a and 107b.

[0007] Here, the etching stopper layer 103 is formed in the etching process for forming Slots 107a and 107b for controlling the depth of these slots 107a and 107b with a sufficient precision. Consequently, the repeatability of resistance of Wiring 108a and 108b can be raised, and the distribution of wiring resistance can be stabilized.

[0008] Moreover, in such multilayer-interconnection structure, the connection which connects wiring and lower layer wiring electrically is formed. The example of the semiconductor device which has the multilayer-interconnection structure where such a connection was formed is shown in drawing 43 . With reference to drawing 43 , a semiconductor device equipped with the multilayer-interconnection structure of having a connection during wiring is explained.

[0009] With reference to drawing 43 , a semiconductor device equipped with the multilayer-interconnection structure of having a connection during the conventional wiring is equipped with the structure fundamentally shown in drawing 42 , and the same structure. However, in drawing 43 , the layer insulation film 104 is formed between the upper wiring 108a and the lower layer wiring 102. the connection for connecting electrically wiring 108a and the lower layer wiring 102 by removing a part of layer insulation film 104 and etching stopper layer 103 by etching -- the hole 109 is formed connection -- the conductor film for connecting electrically wiring 108a and the lower layer wiring 102 is formed in the interior of a hole 109

[0010] As a process for forming the connection during such wiring, the technique called dual DAMASHIN method (the dual damascene method) is indicated by Symposium on VLSI Technology Digest of Technical Papers pp.31-32 (1997).

[0011]

[Problem(s) to be Solved by the Invention] Thus, in the semiconductor device which has

the multilayer-interconnection structure shown in drawing 42 and 43, the amount of [which consist of a silicon nitride between Wiring 108a and 108b and the lower layer wiring 102a and 102b / 103a and 103b] etching stopper layer exists with reference to drawing 42 . The specific inductive capacity of the silicon nitride used as such an etching stopper layer 103 is larger than the silicon oxide used for the layer insulation film 101 etc. For this reason, the capacity between wiring between Wiring 108a and 108b and the lower layer wiring 102a and 102b was increasing. Consequently, RC delay with Wiring 108a and 108b and the lower layer wiring 102a and 102b became large, and the problem that the working speed of a semiconductor device fell had occurred.

[0012] Moreover, since etching stopper layer part 103c existed among Wiring 108a and 108b, the capacity between wiring between Wiring 108a and 108b increased similarly, RC delay of Wiring 108a and 108b became large as a result, and the problem that this speed of a semiconductor device fell had occurred. Such a problem was similarly generated in the semiconductor device equipped with the multilayer-interconnection structure of having the connection structure during the wiring shown in drawing 43 .

[0013] Moreover, as shown in drawing 44 , with detailed-izing of a semiconductor device, the capacity during wiring increases and it has been a big problem. Drawing 44 is Advanced Metallization. for ULSIApplications in 1993 (MATERIALS RESEARCH SOCIETY) p.24 It is the graph which showed the relation between the total capacity during the shown wiring, and a design rule. It turns out that the total capacity during wiring increases at an increasing tempo as a design rule becomes small with reference to drawing 44 .

[0014] It is offering the semiconductor device which it is made in order that this invention's may solve such a technical problem, and one purpose of this invention prevents increase of the capacity during wiring, and can prevent the fall of a working speed.

[0015] Another purpose of this invention is offering the manufacture method of the semiconductor device which increase of the capacity during wiring is prevented and can prevent the fall of a working speed.

[0016]

[Means for Solving the Problem] The semiconductor device in a claim 1 is equipped with an electric conduction field, the 1st and 2nd insulator layers, a covering film, and a wiring layer. The 1st insulator layer is formed on an electric conduction field. The covering film which has the 1st field and 2nd field is formed on the 1st insulator layer. The 2nd insulator layer which has a slot on the 1st field is formed on a covering film. A wiring layer is formed in the interior of a slot. The thickness of the covering film in the

1st field is thinner than the thickness of the covering film in the 2nd field.

[0017] For this reason, in invention according to claim 1, the thickness of the covering film in the 1st field located between an electric conduction field and a wiring layer is thinner than the thickness of the covering film in the 2nd field. Thereby, when using material with larger specific inductive capacity than the 1st and 2nd insulator layers etc. as a covering film, the capacity between an electric conduction field and a wiring layer can prevent a bird clapper greatly. Thereby, RC delay of a wiring layer can prevent a bird clapper greatly. Consequently, it can prevent that the working speed of a semiconductor device falls.

[0018] Moreover, in the etching process for forming the slot in the manufacturing process of this semiconductor device, some covering films in the 1st field are continuously removable by etching for forming a slot by adjusting the process conditions of etching. Consequently, it becomes possible to reduce the capacity between an electric conduction field and a wiring layer, without making the number of manufacturing processes, and mask number of sheets increase conventionally.

[0019] Moreover, since a covering film exists under a wiring layer in this way, when the material which is easy to diffuse in the 1st insulator layer is used as a material of a wiring layer, diffusion into the 1st insulator layer of the material of this wiring layer can be prevented. For example, when the silicon nitride as a covering film exists copper as a material of a wiring layer by the case where the silicon oxide was used as a material of the 1st insulator layer, and a silicon nitride is used as a covering film, respectively, the diffusion to a copper silicon oxide can be prevented effectively.

[0020] Moreover, generally, in case a wiring layer is formed, it has prevented that the material of a wiring layer is spread in the 1st and 2nd insulator layers from the base and the side of a slot by forming barrier metal in the interior of a slot using PVD (the Physical VaporDeposition method). However, since the barrier metal formed of PVD was inferior to other methods in the coverage in the corner of a slot, the material of wiring layers, such as copper, might be spread from this corner. Also in this case, when a covering film exists in the 1st field, diffusion of the material of the wiring layer from this corner can be prevented effectively.

[0021] Moreover, in order to improve the coverage of the film formed of PVD, a long slow spatter, a collimation spatter, the IMP method (the Ionized Metal Plasma method), etc. for having given directivity are used for the particle which carries out incidence to a substrate now. However, by these methods, since directivity is in the particle which carries out incidence to a substrate, the membrane formation to the side of a slot is difficult, the thickness of the barrier metal in the side of a slot becomes thin, and there

are problems, like the membraneous quality is also inferior. In such a case, the material of a wiring layer might be spread in the 2nd insulator layer from the side of this slot. However, since the covering film is formed in the bottom of a wiring layer also in such a case, it can prevent that the material of a wiring layer is spread in the 1st insulator layer out of the 2nd insulator layer. For this reason, it can prevent that the material of a wiring layer is spread in the structure where it is located under an electric conduction field, or a semiconductor substrate.

[0022] The semiconductor device in a claim 2 is equipped with an electric conduction field, the 1st and 2nd insulator layers, a covering film, and a wiring layer. The 1st insulator layer is formed on an electric conduction field. The covering film which has the breakthrough to which the front face of the 1st insulator layer is exposed is formed on the 1st insulator layer. The 2nd insulator layer which has the slot into which the front face of the 1st insulator layer is exposed is formed on a breakthrough. A wiring layer is formed in the interior of a slot.

[0023] For this reason, in invention according to claim 2, a covering film does not exist between an electric conduction field and a wiring layer. When using material, such as a silicon nitride by this with bigger specific inductive capacity than the silicon oxide used as an insulator layer, as a covering film, the capacity between an electric conduction field and a wiring layer can prevent a bird clapper greatly. For this reason, RC delay of a wiring layer can prevent a bird clapper more effectively greatly. Consequently, it can prevent that the working speed of a semiconductor device falls.

[0024] In the composition of claims 1 or 2, as for the semiconductor device in a claim 3, a slot includes the 2nd slot formed by separating this the 1st slot and distance from the 1st slot. A wiring layer contains the 1st wiring layer and the 2nd wiring layer which were formed in the interior of the 1st slot and the 2nd slot, respectively. The field located between the 1st and 2nd slots includes the field in which the covering film is not formed.

[0025] For this reason, in invention according to claim 3, when using material, such as a silicon nitride with bigger specific inductive capacity than the silicon oxide usually used as a layer insulation film, as a covering film, in addition to the capacity between the 1st and 2nd wiring and electric conduction fields, the increase can be prevented also about the capacity between the 1st and the 2nd wiring. Thereby, it originates in the increase in the capacity during the 1st and 2nd wiring, and the 1st and RC delay of the 2nd wiring can prevent a bird clapper more effectively greatly. Consequently, it can prevent that the working speed of a semiconductor device falls. Here, with detailed-izing of a semiconductor device, the capacity during the 1st and 2nd wiring tends to increase, and

does so an effect with an especially remarkable this invention in such a semiconductor device that turned minutely.

[0026] The semiconductor device in a claim 4 is equipped with an insulator layer, the 1st and 2nd covering films, and the 1st and 2nd wiring layers. The 1st covering film is formed on the insulator layer. On an insulator layer, the 1st covering film and interval are separated and the 2nd covering film is formed. The 1st and 2nd wiring layers are formed on the 1st and 2nd covering films, respectively.

[0027] For this reason, in invention according to claim 4, when using the silicon nitride which is material with bigger specific inductive capacity than the silicon oxide conventionally used as an insulator layer as a covering film, the capacity during the 1st and 2nd wiring can prevent a bird clapper greatly. Thereby, it originates in increase of the capacity during the 1st and 2nd wiring, and RC delay can prevent a bird clapper greatly. Consequently, it can prevent that the working speed of a semiconductor device falls. Here, with detailed-izing of a semiconductor device, the capacity during the 1st and 2nd wiring tends to increase, and does so an effect with an especially remarkable this invention in such a semiconductor device that turned minutely.

[0028] Moreover, since the 1st and 2nd covering films exist under the 1st and 2nd wiring layers, respectively, when the material which is easy to diffuse in an insulator layer is used as a material of the 1st and 2nd wiring layers, diffusion of the material of the 1st and 2nd wiring layers can be prevented with these the 1st and 2nd covering films. For example, when the silicon nitride as a covering film exists copper as a material of the 1st and 2nd wiring layers by the case where the silicon oxide was used as a material of an insulator layer, and a silicon nitride is used as a covering film, respectively, the diffusion to a copper silicon oxide can be prevented effectively.

[0029] Moreover, generally, in case a wiring layer is formed, it has prevented that the material of a wiring layer is spread in an insulator layer by using PVD (the Physical Vapor Deposition method) for the field located in the front face of a wiring layer, and forming barrier metal. However, since the barrier metal formed of PVD was inferior to other methods in the coverage in the corner of the 1st and 2nd wiring layers, the material of wiring layers, such as copper, might be spread from this corner. Also in this case, when the 1st and 2nd covering films exist, diffusion of the material of the 1st from this corner and 2nd wiring layers can be prevented effectively. The semiconductor device in a claim 5 is further equipped with the conductor film which connects electrically an electric conduction field, and the 1st wiring layer and electric conduction field in the composition of a claim 4. The electric conduction field is formed in the bottom of an insulator layer. the field located under the 1st wiring layer -- setting -- the

1st covering film and insulator layer -- connection -- the hole is formed connection -- the conductor film is formed in the interior of a hole

[0030] The semiconductor device in a claim 6 is further equipped with an up insulator layer in the composition of claims 4 or 5. The up insulator layer is formed on the 1st and 2nd covering films. The 1st and 2nd slots are formed in the field located on the 1st and 2nd covering films at an up insulator layer, respectively. The 1st and 2nd wiring layers are formed in the interior of the 1st and 2nd slots, respectively.

[0031] The semiconductor device in a claim 7 is the silicon nitride in which a covering film contains a silicon nitride, a silicon oxidization nitride, and a fluorine in the composition of any 1 term of claims 1-6, a silicon oxidization nitride containing a fluorine, and aluminum 2O3. aluminum 2O3 containing a film and a fluorine At least one chosen from the group which consists of a film is included.

[0032] The semiconductor device in a claim 8 contains at least one chosen from the group which is attained to claim 1-3 and a wiring layer and an electric conduction field become from Cu, Cu alloy, aluminum, aluminum alloy, Ag, Ag alloy, Au, W, WN and TiN, TiWN, Ta and TaN, and a doped polysilicon in the composition of any 1 term of 5.

[0033] As for the semiconductor device in a claim 9, the barrier metal layer is formed in the front face of a wiring layer in the composition of any 1 term of claims 1-8.

[0034] For this reason, in invention according to claim 9, when Cu etc. is used as a material of a wiring layer, it can prevent that wiring materials, such as Cu, are spread in the 1st and 2nd insulator layers etc.

[0035] The semiconductor device in a claim 10 contains at least one chosen from the group which a barrier metal layer becomes from the nitride of the alloy containing the nitride of a refractory metal and a refractory metal, the nitride of a refractory metal and silicon, and two or more kinds of refractory metals, and the alloy containing two or more kinds of refractory metals in the composition of a claim 9.

[0036] An electric conduction field is formed by the manufacture method of the semiconductor device in a claim 11. The 1st insulator layer is formed on an electric conduction field. A covering film is formed on the 1st insulator layer. The 2nd insulator layer is formed on a covering film. The slot which exposes the front face of a covering film to the 2nd insulator layer is formed by etching. In the bottom of a slot, etching removes some covering films. A wiring layer is formed in the interior of a slot.

[0037] For this reason, in invention according to claim 11, thickness of a covering film located between an electric conduction field and a wiring layer can be made thinner than before. When using material, such as a silicon nitride by this with bigger specific inductive capacity than the silicon oxide used by carrying out a layer insulation film

conventionally, as a covering film, the capacity between an electric conduction field and a wiring layer can prevent a bird clapper greatly. Consequently, a semiconductor device with it can be obtained easily. [able for RC delay of a wiring layer to be able to prevent a bird clapper effectively greatly, and to prevent the fall of a working speed]

[0038] Moreover, in the etching process for forming a slot, some covering films are continuously removable by adjusting the process conditions of the etching process which forms a slot. Consequently, the semiconductor device which reduced the capacity between an electric conduction field and a wiring layer conventionally can be obtained more easily, without making the number of manufacturing processes increase.

[0039] An electric conduction field is formed by the manufacture method of the semiconductor device in a claim 12. The 1st insulator layer is formed on an electric conduction field. A covering film is formed on the 1st insulator layer. The 2nd insulator layer is formed on a covering film. The slot which exposes the front face of a covering film to the 2nd insulator layer is formed by etching. In the bottom of a slot, etching removes a covering film so that the front face of the 1st insulator layer may be exposed. A wiring layer is formed in the interior of a slot.

[0040] For this reason, in invention according to claim 12, a covering film does not exist between an electric conduction field and a wiring layer. When material, such as a silicon nitride by this with bigger specific inductive capacity than the silicon oxide conventionally used as an insulator layer, is used as a covering film, the capacity between an electric conduction field and a wiring layer can prevent a bird clapper more effectively greatly. Consequently, a semiconductor device with it can be obtained easily. [able for RC delay of a wiring layer to prevent a bird clapper greatly, and to prevent the fall of a working speed]

[0041] An insulator layer is formed by the manufacture method of the semiconductor device in a claim 13. The 1st covering film is formed on an insulator layer. On an insulator layer, the 1st covering film and interval are separated and the 2nd covering film is formed. The 1st and 2nd wiring layers are formed on the 1st and 2nd covering films, respectively.

[0042] For this reason, in invention according to claim 13, a covering film does not exist between the 1st wiring layer and the 2nd wiring layer. When using material, such as a silicon nitride by this with bigger specific inductive capacity than the silicon oxide used as an insulator layer, as a covering film, the capacity between the 1st and 2nd wiring layers can prevent a bird clapper greatly. Consequently, the semiconductor device which RC delay of the 1st and 2nd wiring layers is prevented effectively, and can prevent the fall of a working speed can be obtained easily.

[0043] The manufacture method of the semiconductor device in a claim 14 forms an electric conduction field in the field located under the 1st [under an insulator layer] wiring layer in a claim 13. the connection to which the front face of an electric conduction field is exposed by removing a part of insulator layer and 1st covering film by etching -- a hole is formed connection -- the conductor film which connects an electric conduction field and the 1st wiring layer electrically is formed in the interior of a hole

[0044] The manufacture method of the semiconductor device in a claim 15 In the process at which the process which forms the 1st and 2nd wiring layers forms an up insulator layer on the 1st and 2nd covering films in a claim 13, and the field located on the 1st and 2nd covering films The process which forms the 1st and 2nd slots in an up insulator layer by etching, and the process which embeds the 1st and 2nd wiring layers to the interior of the 1st and 2nd slots, respectively are included. Moreover, an electric conduction field is formed in the field located under the 1st wiring layer under an insulator layer. Opening is formed by removing a part of 1st covering film by etching. the connection to which the front face of an electric conduction field is exposed by removing an insulator layer by etching by using as a mask the 1st covering film which has opening -- a hole is formed connection -- the conductor film which connects an electric conduction field and the 1st wiring layer electrically is formed in the interior of a hole the process which forms the 1st slot, and connection -- the process which forms a hole is continuously performed in one process The process which embeds the 1st wiring layer, and the process which forms a conductor film are continuously performed in one process.

[0045]

[Embodiments of the Invention] Hereafter, the form of operation of this invention is explained based on a drawing.

[0046] (Form 1 of operation) Drawing 1 is the cross section of the semiconductor device by the form 1 of operation of this invention. With reference to drawing 1 , the semiconductor device by the form 1 of operation of this invention is explained.

[0047] With reference to drawing 1 , the semiconductor device by the form 1 of operation of this invention is equipped with Wiring 8a and 8b, the lower layer wiring 2a and 2b, the etching stopper layer 3, and the layer insulation films 1, 6a-6c. The lower layer wiring 2a and 2b is formed on a semiconductor substrate (not shown). The layer insulation film 1 is formed on lower layer wiring 2a and 2b. The etching stopper layer 3 is formed on the layer insulation film 1. The layer insulation films 6a-6c are formed on the etching stopper layer 3. By removing a part of layer insulation film 6a-6c and etching stopper layer 3, the slots 7a and 7b for forming Wiring 8a and 8b are formed.

The barrier metal layers 12a and 12b are formed in the interior of Slots 7a and 7b. A titanium nitride etc. is used as these barrier metal layers 12a and 12b. And the wiring 8a and 8b which consists of conductor films, such as copper, is formed on barrier metal layer 12a and 12b.

[0048] Here, the etching stopper layer 3 does not exist between Wiring 8a and 8b and the lower layer wiring 2a and 2b. When this uses material, such as a silicon nitride with bigger specific inductive capacity than a silicon oxide, as this etching stopper layer 3, the capacity between Wiring 8a and 8b and the lower layer wiring 2a and 2b can prevent a bird clapper greatly. Consequently, RC delay of Wiring 8a and 8b and the lower layer wiring 2a and 2b can prevent a bird clapper effectively greatly. Thereby, it can prevent effectively that the working speed of a semiconductor device falls.

[0049] moreover, the case where copper etc. is used as a material of Wiring 8a and 8b since the barrier metal layers 12a and 12b were formed -- this copper -- layer insulation film 6a- it can prevent being spread in 6c and 1 effectively

[0050] Here, although the wiring formed using the DAMASHIN method like Wiring 8a and 8b may be used for the lower layer wiring 2a and 2b, the electric conduction field in the main front face of the wiring obtained by forming films, such as aluminum and a doped polysilicon, on a layer insulation film as usual or a semiconductor substrate etc. is available for it.

[0051] Drawing 2 - drawing 5 are the cross sections for explaining the manufacturing process of the semiconductor device by the form 1 of operation of this invention shown in drawing 1 . With reference to drawing 2 - drawing 5 , the manufacturing process of the semiconductor device by the form 1 of operation of this invention is explained below.

[0052] First, as shown in drawing 2 , the lower layer wiring 2a and 2b is formed on a semiconductor substrate (not shown). The layer insulation film 1 is formed on lower layer wiring 2a and 2b. The thickness on lower layer wiring 2a of the layer insulation film 1 and 2b is about 0.5-1.5 micrometers. Generally as this layer insulation film 1, they are a plasma TEOS film and plasma SiO2. A film is used. However, recently, it is SiO2. It compares and a fluorine addition silicon oxide with low specific inductive capacity, an SOG film, polymer, etc. are used. By using such a fluorine addition silicon oxide, the capacity between Wiring 8a and 8b and the lower layer wiring 2a and 2b can be reduced further. When using material with such low specific inductive capacity, a laminating is carried out to SiO2 film and it may be used.

[0053] Moreover, when material to which oxidization advances to the interior like copper as lower layer wiring 2a and 2b is used, an antioxidizing film may be formed on the front face of these lower layer wiring 2a and 2b. As this antioxidizing film, insulator

layers and metal membranes, such as a silicon nitride, are used.

[0054] Next, the etching stopper layer 3 is formed on the layer insulation film 1. The silicon nitride formed by the plasma CVD method as an etching stopper layer 3 is used. Moreover, they are a silicon oxidization nitride and aluminum 2O3 in addition to a silicon nitride. A film can also be used.

[0055] Here, specific inductive capacity, such as a silicon nitride used for the etching stopper layer 3, shows a value higher than the specific inductive capacity of the silicon oxide usually used for a layer insulation film etc. For this reason, aluminum 2O3 which contains the silicon nitride which contains a fluorine as an etching stopper layer 3, the silicon oxidization nitride containing a fluorine, and a fluorine in order to reduce the specific inductive capacity of the etching stopper layer 3 You may use a film. The specific inductive capacity of such material is shown in Table 1.

[0056]

[Table 1]

[0057] The thickness of the etching stopper layer 3 is decided by the selection ratio to the layer insulation film 6 of the etching stopper layer 3 in the etching process which forms the slots 7a and 7b (refer to drawing 1) mentioned later. For example, when a plasma SiN film (silicon nitride) is used as a plasma TEOS film and an etching stopper layer 3 as a layer insulation film 6 formed on this etching stopper layer 3, the thickness of the etching stopper layer 3 is about 50-200nm.

[0058] Here, an operation of the silicon nitride as an etching stopper layer 3 can be explained as follows. In plasma, etching gas (C4 F8) is decomposed and the competitive reaction of etching of an insulator layer (a silicon oxide, silicon nitride) and the deposition of a product occurs. An etching rate is determined by the balance of these reactions. Being [consequently] easy to produce the deposition of a product on a silicon nitride, on a silicon nitride, an etching rate becomes small. Moreover, if the rate by which carbon is contained in etching gas or addition gas is high, the rate a product carries out [a rate] a deposition will become high. In the gestalt 1 of operation of this invention, although C4 F8 were used as etching gas, what has a carbonaceous rate high as etching gas is desirable. Moreover, a bigger effect is acquired by adding the gas containing carbon.

[0059] The example of the conditions of the above-mentioned etching process in this case is shown in Table 2.

[0060]

[Table 2]

[0061] Moreover, the etch rate of the various material used as layer insulation films 1 and 6 is shown in Table 3.

[0062]

[Table 3]

[0063] Moreover, the selection ratio to the etch rate and Plasma TEOS of the various material used for the etching stopper layer 3 is shown in Table 4.

[0064]

[Table 4]

[0065] Moreover, when polymer is used as a layer insulation film 6, in the etching stopper layer 3, they are a plasma TEOS film and plasma SiO2. A film, a fluoridation silicon oxide, an SOG film, etc. can be used. In this case, it is Ar/O2 as etching gas of the polymer which constitutes the layer insulation film 6. If it uses, the selection ratio of polymer to the etching stopper layer 3 can be mostly made into infinity. The example of the conditions of the etching process in this case is shown in Table 5.

[0066]

[Table 5]

[0067] Next, the layer insulation film 6 is formed on the etching stopper layer 3. The thickness of this layer insulation film 6 corresponds to the height of Wiring 8a and 8b (refer to drawing 1), and is about 0.3-2.0 micrometers.

[0068] Next, the register spa turns 11a-11c (refer to drawing 3) are formed on the layer insulation film 6. Using this resist pattern as a mask, by removing the layer insulation film 6, as shown in drawing 3 , Slots 7a and 7b are formed.

[0069] In the etching process for forming these slots 7a and 7b, in order to prevent that the etching stopper layer 3 will be removed, it is necessary to enlarge the selection ratio to the etching stopper layer 3 of the layer insulation film 6. Moreover, the width of face of Slots 7a and 7b changes with uses of the wiring 8a and 8b (refer to drawing 1) formed. And in the semiconductor device which has multilayer-interconnection structure, the

width of face changes with wiring also in the interior of each class or the same layer. Usually, when considering the manufacturing process of a semiconductor device, in the wiring formed in the interior of the same layer, it is realistic to consider what has narrow wiring width of face most. And as the minimum width of face of this wiring, the value of about 0.18-1 micrometer is used. Moreover, the aspect ratio of the slots 7a and 7b for forming such wiring is one to about two. Henceforth, the width of face of Wiring 8a and 8b explains the case where it is referred to as about 0.18-1 micrometer as mentioned above.

[0070] Next, as shown in drawing 4 , in the pars basilaris ossis occipitalis of Slots 7a and 7b, etching removes the etching stopper layer 3.

[0071] As a method of removing the etching stopper layer 3, wet etching and RIE (Reactive Ion Etching) are mentioned. The conditions of wet etching at the time of using a silicon nitride as an etching stopper layer 3, and using a silicon oxide as a layer insulation film 6 are shown in Table 6.

[0072]

[Table 6]

[0073] In wet etching, a silicon nitride can be **********ed very alternatively.

[0074] Moreover, the conditions of RIE are shown in Table 7.

[0075]

[Table 7]

[0076] In RIE, the selection ratio to the silicon nitride of a silicon oxide can be enlarged by enlarging the radical component in plasma. This is for etching by chemical operation to tend to advance according to combination of a silicon nitride being chemically unstable compared with combination of a silicon oxide.

[0077] Next, as shown in drawing 5 , the barrier metal layer 12 is formed the interior of Slots 7a and 7b, and on layer insulation film 6a - 6c. TiN, WN, TaN, etc. can be used as this barrier metal layer 12. And as the formation method of this barrier metal layer 12, the PVD (Physical Vapor Deposition) method and the CVD (Chemical Vapor Deposition) method are mentioned. In PVD, you may use the collimation spatter which has improved the directivity of the particle which carries out incidence to a substrate in addition to the usual spatter, a long slow spatter, the IMP method (indicated by the Ionized Metal Plasma method, for example, Peijun Ding, et al, and VMIC Conference

pp.87-92 (1997)), etc.

[0078] Next, the conductor films 8, such as copper (Cu) used as Wiring 8a and 8b, are formed on the barrier metal layer 12. As the formation method of the copper used as this conductor film 8, PVD, CVD, and the galvanizing method are mentioned, for example. Since the coverage of the film formed of PVD is not good when PVD is used, it is difficult to embed copper to the interior of Slots 7a and 7b generally. For this reason, after forming the copper which makes substrate temperature high, how to carry out a reflow of the copper by making ambient temperature into an elevated temperature is taken. By using together the spatter which has improved such a method and directivity, copper can be embedded in an about 1.5-aspect ratio slot.

[0079] On the other hand, when CVD and the galvanizing method are used as the formation method of this copper, a good embedded property is acquired.

[0080] Here, the membrane formation conditions for every various material by the spatter which is one of the PVD are shown in Table 8.

[0081]

[Table 8]

[0082] Moreover, the membrane formation conditions for every various material at the time of using CVD are shown in Table 9.

[0083]

[Table 9]

[0084] Moreover, the membrane formation conditions of the copper at the time of using the galvanizing method are shown in Table 10.

[0085]

[Table 10]

[0086] Here, the adhesion good as a property and diffusion prevention capacity which are required of the barrier metal layer 12 are mentioned. The nitride of the alloy which consists of two or more kinds of refractory metals, the alloy which consists of refractory metals, such as a nitride of refractory metals, such as refractory metals, such as Cr, Ta, and W, and CrN, MoN, TiSiN, WSiN, and TaSiN, and two or more kinds of refractory metals, the nitride of silicon, TiW, etc., as a material which fills such a demand in

addition to the above-mentioned material, TiWN, etc., is mentioned; and the barrier metal layer 12 may be formed by such material.

[0087] Moreover, as a material of the conductor film 8 used as Wiring 8a and 8b, you may use a refractory metal called a doped polysilicon, W, WN and TiN, TiWN, and TaN excellent in the lows Cu, Ag, and Au of electric resistance, aluminum alloys (AlCu, AlSiCu, etc.), and thermal resistance, or its compound. Here, if it forms the conductor film 8 by the same material as the material which constitutes the above-mentioned barrier metal layer 12 in using a refractory metal or its compound, the number of manufacturing processes is reducible.

[0088] Next, the conductor film 8 and the barrier metal layer 12 which were formed on layer insulation film 6a - 6c are removed using the chemical machinery grinding method (the CMP method). Thus, the structure shown in drawing 1 can be acquired.

[0089] Here, as a slurry used for the CMP method, the mixed liquor of QCTT1010 and H202 of Rodel, Inc. can be used, for example. Moreover, as a pad used in this CMP method, the laminating pad of IC1000/SUBA400 of Rodel, Inc. can be used.

[0090] Moreover, it is also possible by repeating such a process to form the multilayer-interconnection structure of having much more layers.

[0091] Drawing 6 is the cross section showing the 1st modification of the semiconductor device by the gestalt 1 of operation of this invention. With reference to drawing 6 , the 1st modification of the semiconductor device by the gestalt 1 of operation of this invention is explained.

[0092] With reference to drawing 6 , the 1st modification of the semiconductor device by the gestalt 1 of operation of this invention is fundamentally equipped with the same structure as the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 . However, in the 1st modification shown in this drawing 6 , the lower layer wiring 2a and 2b is wiring of the flush type formed by the DAMASHIN method. It can do [using copper etc. or] as a component of these lower layer wiring 2a and 2b. And on these lower layer wiring 2a and 2b and the layer insulation film 1, the covering film 5 which consists of a silicon nitride for preventing oxidization of the lower layer wiring 2a and 2b is formed. Between the covering film 5 and Wiring 8a and 8b, the layer insulation film 4 which consists of a silicon oxide is formed.

[0093] Thus, the same effect as the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 can be acquired also by the case of the wiring the lower layer wiring 2a and 2b was formed by the DAMASHIN method.

[0094] Drawing 7 is the cross section showing the 2nd modification of the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 . With reference

to drawing 7 , the 2nd modification of the semiconductor device by the gestalt 1 of operation of this invention is fundamentally equipped with the same structure as the 1st modification of the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 6 . However, in the 2nd modification shown in this drawing 7 , the covering films 5a and 5b which consist of a silicon nitride are formed in the field located on lower layer wiring 2a and 2b. For this reason, the field in which the covering film which consists of a silicon nitride is not formed exists in the field located among the lower layer wiring 2a and 2b.

[0095] For this reason, even when a silicon nitride with larger specific inductive capacity than a silicon oxide etc. is used as covering films 5a and 5b, the capacity between the lower layer wiring 2a and 2b can prevent a bird clapper greatly. Thereby, increase of RC delay in the lower layer wiring 2a and 2b can be suppressed.

[0096] Moreover, the capacity during wiring by the gestalt 1 of operation of this invention obtained as mentioned above is shown in Table 11 with the example of comparison.

[0097] in addition, as structure which measured the data shown in this table 11 With reference to drawing 1 , as for the bottom of about 1 micrometer and the layer insulation film 1, the interval whose thickness the width of face of Wiring 8a and 8b is 0.3 micrometers, and is between 0.6 micrometers, wiring 8a, and 8b serves as a semiconductor substrate, and the thickness of 0.3 micrometers and the layer insulation film 1 used the structure (one layer structure) where the lower layer wiring 2a and 2b did not exist. Moreover, the capacity between wiring and a semiconductor substrate is also contained in the capacity during the wiring shown in Table 11, and the capacity during vertical wiring is evaluated using the capacity between Wiring 8a and 8b and a semiconductor substrate.

[0098]

[Table 11]

[0099] As shown in Table 11, it turns out that the capacity during wiring can be reduced by this invention.

[0100] (Gestalt 2 of operation) Drawing 8 is the cross section of the semiconductor device by the gestalt 2 of operation of this invention. With reference to drawing 8 , the semiconductor device by the gestalt 2 of operation of this invention is explained.

[0101] With reference to drawing 8 , the semiconductor device by the gestalt 2 of operation of this invention is fundamentally equipped with the same structure as the

semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 . However, in the semiconductor device by the gestalt 2 of operation of this invention shown in drawing 8 , the etching stopper layers 3a and 3b remain under Wiring 8a and 8b. And the thickness of the etching stopper layers 3a and 8b located under this wiring 8a and 8b is thinner than the thickness of the etching stopper layer 3 located between wiring 8a and wiring 8b.

[0102] For this reason, in the semiconductor device by the gestalt 2 of operation of this invention shown in drawing 8 , even when material, such as a silicon nitride with bigger specific inductive capacity than a silicon oxide, is used as an etching stopper layer 3, the capacity between Wiring 8a and 8b and the lower layer wiring 2a and 2b can be reduced. Consequently, RC delay with Wiring 8a and 8b and the lower layer wiring 2a and 2b can prevent a bird clapper greatly, and can prevent the fall of the working speed of a semiconductor device.

[0103] Moreover, in the etching process for forming the slots 7a and 7b in the manufacturing process mentioned later, a part of etching stopper layer 3 is continuously removable by etching which forms Slots 7a and 7b in the bottom of Slots 7a and 7b by adjusting the process conditions of etching. Thereby, without making the number of manufacturing processes increase, thickness of the etching stopper layers 3a and 3b located under wiring 8a and 8b can be made thin, and the capacity between Wiring 8a and 8b and the lower layer wiring 2a and 2b can be reduced.

[0104] Drawing 9 and 10 are the cross sections for explaining the manufacturing process of the semiconductor device by the form 2 of operation of this invention shown in drawing 8 . With reference to drawing 9 and 10, the manufacturing process of the semiconductor device by the form 2 of operation of this invention is explained below.

[0105] First, after carrying out the manufacturing process of the semiconductor device by the form 1 of operation of this invention shown in drawing 2 , the resist patterns 11a-11c (refer to drawing 9) are formed on the layer insulation film 6 (refer to drawing 2). And as shown in drawing 9 , Slots 7a and 7b are formed by removing the layer insulation film 6 by using the resist patterns 11a-11c as a mask. At this time, a part of etching stopper layer 3 is continuously removed in the etching process which forms Slots 7a and 7b by adjusting the process conditions of etching in the etching process which forms these slots 7a and 7b.

[0106] Thus, thickness of the etching stopper layers 3a and 3b located under wiring 8a and 8b can be made thin, without increasing the number of manufacturing processes, since a part of etching stopper layer 3 is continuously removed in the etching process which forms Slots 7a and 7b.

[0107] In addition, completely different conditions from the conditions of the etching process for forming Slots 7a and 7b like the manufacturing process which showed the process which removes a part of etching stopper layer 3 here to drawing 4 of the semiconductor device by the form 1 of operation of this invention may perform as another process.

[0108] Next, as shown in drawing 10 , the conductor film 8 used as Wiring 8a and 8b (refer to drawing 8) is formed the interior of Slots 7a and 7b, and on layer insulation film 6a - 6c. Under the present circumstances, you may form a barrier metal layer like the form 1 of operation of this invention the interior of Slots 7a and 7b, and on layer insulation film 6a - 6c.

[0109] Then, structure as shown in drawing 8 can be easily acquired by removing the conductor film 8 located on layer insulation film 6a - 6c using the CMP method etc.

[0110] (Form 3 of operation) Drawing 11 is the cross section showing the semiconductor device by the form 3 of operation of this invention. With reference to drawing 11 , the semiconductor device by the form 3 of operation of this invention is explained.

[0111] With reference to drawing 11 , the semiconductor device by the form 3 of operation of this invention is equipped with Wiring 8a and 8b, the lower layer wiring 2a and 2b, the layer insulation films 1, 6a-6c, and the etching stopper layers 3c and 3d. The lower layer wiring 2a and 2b is formed on a semiconductor substrate (not shown). The layer insulation film 1 which consists of a silicon oxide is formed on lower layer wiring 2a and 2b. On the layer insulation film 1, a predetermined interval is separated and the etching stopper layers 3c and 3d are formed. The material same as the these etching stopper layers [3c and 3d] quality of the material as the etching stopper layer in the semiconductor device by the form 1 of operation of this invention can be used. On the layer insulation film 1 and the etching stopper layers 3c and 3d, the layer insulation films 6a-6c are formed. Slots 7a and 7b are formed in the field located on etching stopper layer 3c and 3d at the layer insulation films 6a-6c. Wiring 8a and 8b is formed in the interior of slot 7a and 7b.

[0112] Thus, since the field where the etching stopper layer is not formed in the field located between wiring 8a and wiring 8b exists, when using material, such as a silicon nitride with bigger specific inductive capacity than a silicon oxide etc., as etching stopper layers 3c and 3d, the capacity between wiring 8a and wiring 8b can prevent a bird clapper greatly. Consequently, it originates in the capacity between Wiring 8a and 8b, RC delay becomes large, and it can prevent that the working speed of a semiconductor device falls.

[0113] Here, it becomes large as wiring makes detailed capacity between adjoining wiring 8a and wiring 8b, and in a submicron field, since the direction of the capacity between contiguity wiring becomes dominant from the capacity between layers in the whole wiring capacity, reduction of the capacity during the contiguity wiring becomes very important.

[0114] Moreover, the capacity during wiring by the form 3 of operation of this invention obtained as mentioned above is shown in Table 12.

[0115]

[Table 12]

[0116] In addition, the structure which measured the data shown in this table 12 is the same as the structure which measured the data fundamentally shown in Table 11. Moreover, the capacity between wiring and a semiconductor substrate is also contained in the capacity during the wiring shown in Table 12.

[0117] Drawing 12 -16 are a cross section for explaining the manufacturing process of the semiconductor device by the form 3 of operation of this invention shown in drawing 11 . Hereafter, with reference to drawing 12 -16, the manufacturing process of the semiconductor device by the form 3 of operation of this invention is explained.

[0118] First, as shown in drawing 12 , the lower layer wiring 2a and 2b is formed on a semiconductor substrate (not shown). The wiring which used the DAMASHIN method like the forms 1 and 2 of operation of this invention may be used for these lower layer wiring 2a and 2b, and the wiring using a conventional doped polysilicon, conventional aluminum, etc. may be used for it, or the electric conduction field formed on the semiconductor substrate is available for it. And the layer insulation film 1 is formed on lower layer wiring 2a and 2b. The etching stopper layer 3 is formed on the layer insulation film 1.

[0119] Next, as shown in drawing 13 , the resist patterns 11d and 11e are formed on the etching stopper layer 3. By using these resist patterns 11d and 11e as a mask, it etches so that the etching stopper layers 3c and 3d may be made to remain to the field located under the field which forms Wiring 8a and 8b (refer to drawing 1). If the margin of the alignment at the time of processing of a slot is taken into consideration here, it is necessary to make width of face of the resist patterns 11d and 11e into the above (margin x2 of the width-of-face + alignment of the slot for wiring) size.

[0120] Next, after removing the resist patterns 11d and 11e, as shown in drawing 14 , the layer insulation film 6 is formed the layer insulation film 1 and on etching stopper

layer 3c and 3d.

[0121] Next, the resist patterns 11a-11c (refer to drawing 15) are formed on the layer insulation film 6. By removing some layer insulation films 6 by using these resist patterns 11a-11c as a mask, as shown in drawing 15 , Slots 7a and 7b are formed.

[0122] Next, after removing the resist patterns 11a-11c, as shown in drawing 16 , the conductor film 8 is formed the interior of Slots 7a and 7b, and on layer insulation film 6a - 6c. After using the various material shown in the gestalt 1 of operation of this invention as this conductor film 8 and forming a barrier metal layer the interior of Slots 7a and 7b, and on layer insulation film 6a - 6c, you may form this conductor film 8.

[0123] Next, the structure shown in drawing 11 is acquired by removing the conductor film 8 located on layer insulation film 6a - 6c using the CMP method etc. Thus, the semiconductor device by the gestalt 3 of operation of this invention can be obtained easily.

[0124] Moreover, the same effect is acquired even if it applies the 1st of a semiconductor device and the 2nd modification by the gestalt 1 of operation of this invention shown in drawing 6 and 7 to the semiconductor device by the gestalt 3 of operation of this this invention.

[0125] Drawing 17 is the cross section showing the modification of the semiconductor device by the gestalt 3 of operation of this invention. With reference to drawing 17 , the modification of the semiconductor device by the gestalt 3 of operation of this invention is fundamentally equipped with the same structure as the semiconductor device by the gestalt 3 of operation of this invention shown in drawing 11 . However, in the modification shown in this drawing 17 , the etching stopper layers [3e and 3f] thickness located under wiring 8a and 8b is thinner than the thickness of an etching stopper layer located in fields other than under wiring 8a and 8b.

[0126] for this reason, in addition to the effect acquired in the semiconductor device by the form 3 of operation of this invention shown in drawing 11 , the modification of the semiconductor device by the form 3 of operation of this invention shown in drawing 17 acquires further the effect acquired in the semiconductor device by the form 2 of operation of this invention shown in drawing 8 , and the same effect -- things are made

[0127] Moreover, in the modification shown in this drawing 17 , even if it applies the structure of the 1st and 2nd modifications by the form 1 of operation of this invention shown in drawing 6 and drawing 7 , the same effect is acquired.

[0128] (Form 4 of operation) Drawing 18 is the cross section of the semiconductor device by the form 4 of operation of this invention. With reference to drawing 18 , the semiconductor device by the form 4 of operation of this invention is explained below.

[0129] With reference to drawing 18 , the semiconductor device by the form 4 of operation of this invention is fundamentally equipped with the same structure as the semiconductor device by the form 3 of operation of this invention shown in drawing 11 . However, in the semiconductor device by the form 4 of operation of this invention shown in this drawing 18 , an etching stopper layer does not exist in the field located under wiring 8a and 8b, but the etching stopper layers 3g-3j remain only on the side of Wiring 8a and 8b.

[0130] for this reason, in addition to the effect acquired in the semiconductor device by the form 3 of operation of this invention shown in drawing 11 , in the semiconductor device by the form 4 of this operation, the effect acquired in the semiconductor device by the form 1 of operation of this invention shown in drawing 1 can be acquired collectively

[0131] Drawing 19 and drawing 20 are the cross sections for explaining the manufacturing process of the semiconductor device by the form 4 of operation of this invention shown in drawing 18 . With reference to drawing 19 and drawing 20 , the manufacturing process of the semiconductor device by the form 4 of operation of this invention is explained below.

[0132] First, after carrying out the 1st process of the manufacturing process of the semiconductor device by the form 3 of operation of this invention shown in drawing 12 - drawing 15 - the 4th process, as shown in drawing 19 , in the bottom of Slots 7a and 7b, etching removes an etching stopper layer.

[0133] Next, after removing the resist patterns 11a-11c, as shown in drawing 20 , the conductor film 8 is formed the interior of Slots 7a and 7b, and on layer insulation film 6a - 6c. Here, before forming the conductor film 8, you may form a barrier metal layer the interior of Slots 7a and 7b, and on layer insulation film 6a - 6c.

[0134] Next, structure as shown in drawing 18 is acquired by removing the conductor film 8 located on layer insulation film 6a - 6c using the CMP method etc. Thus, the semiconductor device by the form 4 of operation of this invention can be obtained easily.

[0135] Moreover, the same effect is acquired even if it applies the structure of the 1st of the semiconductor device by the form 1 of operation of this invention shown in the semiconductor device by the form 4 of this operation at drawing 6 and drawing 7 , and the 2nd modification.

[0136] (Form 5 of operation) Drawing 21 is the cross section of the semiconductor device by the form 5 of operation of this invention. With reference to drawing 21 , the semiconductor device by the form 5 of operation of this invention is explained below.

[0137] With reference to drawing 21 , the semiconductor device by the gestalt 5 of operation of this invention is fundamentally equipped with the same structure as the

semiconductor device by the gestalt 3 of operation of this invention shown in drawing 11 . However, in the semiconductor device by the gestalt 5 of operation of this invention shown in this drawing 21 , the layer insulation films 4a and 4b which consist of a silicon oxide are formed between the lower layer wiring 2 and Wiring 8a and 8b. And opening 10 is formed in the etching stopper layers 3k and 3l. located under wiring 8a. moreover, the field located under wiring 8a -- setting -- the layer insulation films 4a and 4b -- connection -- the hole 9 is formed this connection -- a hole -- wiring layer 8a and the lower layer wiring 2 are electrically connected by the conductor film formed in the 9 interior

[0138] Thus, also in the semiconductor device by the gestalt 5 of operation of this invention, since the field where the etching stopper layer is not formed between wiring 8a and wiring 8b exists, the same effect as the semiconductor device by the gestalt 3 of operation of this invention shown in drawing 11 can be acquired.

[0139] Drawing 22 and drawing 23 are the cross sections for explaining the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 . With reference to drawing 22 and drawing 23 , the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention is explained below.

[0140] First, as shown in drawing 22 , the lower layer wiring 2 is formed by forming a slot in the layer insulation film 1, embedding a conductor film in this slot, and removing the conductor film located on the layer insulation film 1 of fields other than this slot using the CMP method etc. Next, the layer insulation film 4 is formed on the lower layer wiring 2 and the layer insulation film 1. An etching stopper layer is formed on the layer insulation film 4. A resist pattern (not shown) is formed on an etching stopper layer, and etching removes a part of etching stopper layer by using this resist pattern as a mask. Thus, 3m of etching stopper layers and the etching stopper layers 3k and 3l. which have opening 10 are formed on the layer insulation film 4. Next, after removing a resist pattern, the layer insulation film 6 is formed on the layer insulation film 4 and the etching stopper layers 3k-3m.

[0141] Next, a resist pattern (not shown) is formed on the layer insulation film 6. The slots 7a and 7b (refer to drawing 23) for forming Wiring 8a and 8b are formed by using this resist pattern as a mask. under the present circumstances, the connection for connecting wiring 8a and the lower layer wiring 2 by using these etching stopper layers 3k and 3l. as a mask, since opening 10 is formed in the etching stopper layers 3k and 3l. -- a hole 9 is formed simultaneously Then, a resist pattern is removed. Thus, structure as shown in drawing 23 is acquired.

[0142] then, Slots 7a and 7b and connection -- after forming a conductor film in the interior of a hole 9, structure as shown in drawing 21 can be acquired by performing the manufacturing process of the semiconductor device in the forms 1-4 of operation of this invention, and the same process Thus, the semiconductor device by the form 5 of operation of this invention can be obtained easily.

[0143] Drawing 24 is the cross section showing the 1st modification of the semiconductor device by the form 5 of operation of this invention. With reference to drawing 24 , the 1st modification of the semiconductor device by the form 5 of operation of this invention is explained.

[0144] With reference to drawing 24 , the 1st modification of the semiconductor device by the form 5 of operation of this invention is fundamentally equipped with the same structure as the form 5 of operation of this invention shown in drawing 21 . However, the covering film 5 which consists of a silicon nitride like the 1st modification of the semiconductor device by the form 1 of operation of this invention shown in drawing 6 is formed in the front face of the layer insulation film 1. Thus, by forming the covering film 5, when using material into which the lower layer wiring 2 oxidizes easily, the lower layer wiring 2 can be protected with this covering film 5.

[0145] Drawing 25 is the cross section showing the 2nd modification of the semiconductor device by the form 5 of operation of this invention. With reference to drawing 25 , the 2nd modification of the semiconductor device by the form 5 of operation of this invention is explained.

[0146] With reference to drawing 25 , the 2nd modification of the semiconductor device by the form 5 of operation of this invention is fundamentally equipped with the same structure as the 1st modification of the semiconductor device by the form 5 of operation of this invention shown in drawing 24 . However, in the 2nd modification shown in drawing 25 , the covering films 5c and 5d are formed only in the field located after the lower layer wiring 2, and the covering film is not formed on the layer insulation film 1 of the field located under wiring 8b. For this reason, when other wiring layers are formed in the field which is located under wiring 8b and located under the layer insulation film 1, the covering film 5 does not exist between other wiring layers and wiring 8b. For this reason, when using material with bigger specific inductive capacity than a silicon oxide like a silicon nitride as covering films 5c and 5d, it can decrease rather than the 1st modification of the semiconductor device by the form 5 of operation of this invention which showed the capacity between other wiring layers and wiring 8b which are formed in the bottom of this layer insulation film 1 to drawing 24 .

[0147] Drawing 26 is the cross section showing the 3rd modification of the

semiconductor device by the form 5 of operation of this invention. With reference to drawing 26 , the 3rd modification of the semiconductor device by the form 5 of operation of this invention is explained below.

[0148] With reference to drawing 26 , the 3rd modification of the semiconductor device by the form 5 of operation of this invention is fundamentally equipped with the same structure as the semiconductor device by the form 5 of operation of this invention shown in drawing 21 . However, in the 3rd modification shown in drawing 26 , etching stopper layer 3r exists between wiring 8a and wiring 8b. Moreover, the etching stopper layers 3s and 3t exist in other fields other than the field in which the wiring 8a and 8b on layer insulation film 4a and 4b is located. And the thickness of etching stopper layer 3r is thinner than etching stopper layers [3k-3m] thickness.

[0149] For this reason, in the 3rd modification of the semiconductor device by the gestalt 5 of operation of this invention, when using material, such as a silicon nitride with larger specific inductive capacity than a silicon oxide etc., as the etching stopper layers 3k-3m and 3r-3t, the capacity between wiring 8a and wiring 8b can prevent a bird clapper greatly. Consequently, it originates in the capacity between Wiring 8a and 8b, RC delay becomes large, and it can prevent that the working speed of a semiconductor device falls.

[0150] Moreover, since the etching stopper layers 3k-3m and 3r-3t are formed so that layer insulation film 4a and 4b top may be covered, when the formation position of Slots 7a and 7b shifts, it can prevent that Slots 7a and 7b reach even the layer insulation films 4a and 4b. Thereby, the good wiring 8a and 8b of a dimensional accuracy can be obtained easily. Moreover, the semiconductor device located under wiring 8a and 8b can prevent receiving an injury by etching for forming these slots 7a and 7b simultaneously. Consequently, the fall of a working speed can be prevented and a reliable semiconductor device can be obtained.

[0151] Drawing 27 -31 are a cross section for explaining the 1st modification of the manufacturing process of the semiconductor device by the form 5 of operation of this invention shown in drawing 21 . With reference to drawing 27 -31, the 1st modification of the manufacturing process of the semiconductor device by the form 5 of operation of this invention is explained below.

[0152] First, as shown in drawing 27 , the lower layer wiring 2 is formed by forming a slot in the layer insulation film 1, embedding a conductor film in this slot, and removing the conductor film located on the layer insulation film 1 of fields other than this slot using the CMP method etc. Next, the layer insulation film 4 is formed on the lower layer wiring 2 and the layer insulation film 1. An etching stopper layer is formed on the layer

insulation film 4. A resist pattern (not shown) is formed on an etching stopper layer, and etching removes a part of etching stopper layer by using this resist pattern as a mask. Thus, the etching stopper layers 3c and 3m are formed on the layer insulation film 4. Next, after removing a resist pattern, the layer insulation film 6 is formed on the layer insulation film 4 and the etching stopper layers 3c and 3m.

[0153] Next, as shown in drawing 28 , the resist patterns 11a and 11b are formed on the layer insulation film 6.

[0154] next, by removing a part of layer insulation film 4 and 6 and etching stopper layer 3c by using the resist patterns 11a and 11b as a mask shows to drawing 29 -- as -- connection -- a hole 9 is formed Then, the resist patterns 11a and 11b are removed.

[0155] Next, as shown in drawing 30 , the resist patterns 11c, 11d, and 11e are formed on layer insulation film 6a and 6b.

[0156] Next, as shown in drawing 31 , the slots 7a and 7b for wiring are formed by etching by using the resist patterns 11c, 11d, and 11e as a mask.

[0157] Then, the resist patterns 11c, 11d, and 11e are removed. then, Slots 7a and 7b and connection -- after forming a conductor film in the interior of a hole 9, structure as shown in drawing 21 can be acquired by performing the manufacturing process of the semiconductor device in the forms 1-4 of operation of this invention, and the same process Thus, the semiconductor device by the form 5 of operation of this invention can be obtained easily.

[0158] Drawing 32 and 33 are the cross sections for explaining the 2nd modification of the manufacturing process of the semiconductor device by the form 5 of operation of this invention shown in drawing 21 . With reference to drawing 32 -33, the 2nd modification of the manufacturing process of the semiconductor device by the form 5 of operation of this invention is explained below.

[0159] First, after carrying out the manufacturing process shown in drawing 27 and 28, as shown in drawing 32 , opening 13 is formed by etching by using the resist patterns 11a and 11b as a mask. Under the present circumstances, the front face of the layer insulation film 4 makes it expose in the bottom of opening 13. Then, the resist patterns 11a and 11b are removed.

[0160] Next, as shown in drawing 33 , the resist patterns 11c, 11d, and 11e are formed on layer insulation film 6a and 6b.

[0161] And the slots 7a and 7b for wiring are formed like drawing 31 by removing the layer insulation films 6a and 6b by etching by using the resist patterns 11c, 11d, and 11e as a mask. in the case of this etching, the etching stopper layers 3k and 3l. act as a mask, and some layer insulation films 4 are removed by etching -- connection -- a hole 9 is

formed

[0162] Then, the resist patterns 11c, 11d, and 11e are removed. then, Slots 7a and 7b and connection -- after forming a conductor film in the interior of a hole 9, structure as shown in drawing 21 can be acquired by performing the manufacturing process of the semiconductor device in the gestalten 1-4 of operation of this invention, and the same process Thus, the semiconductor device by the gestalt 5 of operation of this invention can be obtained easily.

[0163] In addition, the 1st of the manufacturing process of a semiconductor device and the 2nd modification by the gestalt 5 of operation of this invention shown in drawing 27 -33 are applicable also to the manufacturing process of the semiconductor device shown in drawing 24 -26.

[0164] (Form 6 of operation) Drawing 34 is the cross section showing the semiconductor device by the form 6 of operation of this invention. With reference to drawing 34 , the semiconductor device by the form 6 of operation of this invention is explained.

[0165] With reference to drawing 34 , the semiconductor device by the form 6 of operation of this invention is fundamentally equipped with the same structure as the semiconductor device by the form 5 of operation of this invention shown in drawing 21 . However, the etching stopper layer is not formed in the field located under wiring 8a and 8b in the semiconductor device by the form 6 of operation of this invention shown in this drawing 34 .

[0166] for this reason, in addition to the effect acquired in the semiconductor device by the form 5 of operation of this invention shown in drawing 21 , in the semiconductor device by the form 6 of operation of this invention shown in drawing 34 , the effect acquired in the semiconductor device by the form 1 of operation of this invention shown in drawing 1 and the same effect can be acquired

[0167] Drawing 35 is a cross section for explaining the manufacturing process of the semiconductor device by the form 6 of operation of this invention shown in drawing 34 . With reference to drawing 35 , the manufacturing process of the semiconductor device by the form 6 of operation of this invention shown below at drawing 34 is explained.

[0168] First, after carrying out the 1st process of the manufacturing process of a semiconductor device and the 2nd process by the form 5 of operation of this invention shown in drawing 22 and drawing 23 , as shown in drawing 35 , in the bottom of Slots 7a and 7b, etching removes an etching stopper layer.

[0169] Then, structure as shown in drawing 34 can be acquired by performing the manufacturing process of the semiconductor device by the form 5 of operation of this

invention, and the same process. Thus, the semiconductor device by the form 6 of operation of this invention can be obtained easily.

[0170] Moreover, the same effect can be acquired even if it applies the 1st of the semiconductor device by the form 5 of operation of this invention shown in drawing 24 - 26 - the 3rd modification to the semiconductor device by the form 6 of operation of this invention shown in this drawing 34 .

[0171] Moreover, you may apply to the manufacturing process of the semiconductor device by the form 6 of operation of this invention which showed the 1st of the manufacturing process of a semiconductor device and the 2nd modification by the form 5 of operation of this invention shown in drawing 27 -33 to this drawing 34 .

[0172] (Form 7 of operation) Drawing 36 is the cross section of the semiconductor device by the form 7 of operation of this invention. With reference to drawing 36 , the semiconductor device by the form 7 of operation of this invention is explained below.

[0173] With reference to drawing 36 , the semiconductor device by the form 7 of operation of this invention is fundamentally equipped with the same structure as the semiconductor device by the form 3 of operation of this invention shown in drawing 11 . However, in the semiconductor device by the form 7 of operation of this invention shown in this drawing 36 , the side of Wiring 8a and 8b and the etching stopper layers [3c and 3d] side are mostly located in a coplanar.

[0174] Thus, also in the semiconductor device by the form 7 of operation of this invention, since the field where the etching stopper layer is not formed between wiring 8a and wiring 8b exists, the same effect as the semiconductor device by the form 3 of operation of this invention shown in drawing 11 can be acquired.

[0175] Moreover, like the semiconductor device shown in drawing 11 , since the etching stopper layers 3c and 3d have not extended outside the side of Wiring 8a and 8b, area of the field in which the etching stopper layer between wiring 8a and 8b is not formed can be made larger than the semiconductor device of drawing 11 . Consequently, the capacity between wiring 8a and 8b can be reduced more effectively.

[0176] Drawing 37 -40 are a cross section for explaining the manufacturing process of the semiconductor device by the form 7 of operation of this invention shown in drawing 36 . With reference to drawing 37 -40, the manufacturing process of the semiconductor device by the form 7 of operation of this invention is explained below.

[0177] First, after carrying out the manufacturing process shown in drawing 12 and 13, as shown in drawing 37 , the layer insulation film 6 is formed on the layer insulation film 1 and the resist patterns 11d and 11e.

[0178] Next, as shown in drawing 38 , the layer insulation film 6 located on resist

pattern 11d and 11e is removed by using the CMP method etc.

[0179] Next, as shown in drawing 39 , the resist patterns 11d and 11e are removed. Thus, the slots 7a and 7b for wiring can be formed.

[0180] For this reason, it differs in the forms 1-6 of operation of this invention, there is no need of performing the etching process which forms Slots 7a and 7b, and there is also no need of forming the resist pattern for this etching. Consequently, the manufacturing process of a semiconductor device can be simplified and a manufacturing cost can be reduced.

[0181] Moreover, since Slots 7a and 7b are formed in the field to which the resist patterns 11d and 11e on etching stopper layer 3c and 3d existed at a self-adjustment target, an etching stopper layer does not exist between wiring 8a and 8b. For this reason, the capacity between wiring 8a and 8b can be reduced more.

[0182] And as shown in drawing 40 after the process shown in drawing 39 , the conductor film 8 is formed the interior of Slots 7a and 7b, and on the layer insulation films 6a and 6b and 6c.

[0183] Structure as shown in drawing 36 can be acquired after it by performing the manufacturing process of the semiconductor device in the forms 1-4 of operation of this invention, and the same process.

[0184] Thus, the semiconductor device by the form 7 of operation of this invention can be obtained easily.

[0185] It should be thought that the form of the operation indicated this time is [no] instantiation at points, and restrictive. The range of this invention is shown by the above-mentioned not explanation but claim, and it is meant that a claim, an equal meaning, and all change in within the limits are included.

[0186]

[Effect of the Invention] As mentioned above, according to invention according to claim 1 to 15, the semiconductor device which can prevent the fall of a working speed can be obtained by reducing the capacity during wiring and suppressing RC delay of wiring.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the cross section of the semiconductor device by the gestalt 1 of operation of this invention.

[Drawing 2] It is a cross section for explaining the 1st process of the manufacturing process of the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 .

[Drawing 3] It is a cross section for explaining the 2nd process of the manufacturing process of the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 .

[Drawing 4] It is a cross section for explaining the 3rd process of the manufacturing process of the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 .

[Drawing 5] It is a cross section for explaining the 4th process of the manufacturing process of the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 .

[Drawing 6] It is the cross section showing the 1st modification of the semiconductor device by the gestalt 1 of operation of this invention shown in drawing 1 .

[Drawing 7] It is the cross section having shown the 2nd modification of the semiconductor device by the gestalt 1 of operation of this invention.

[Drawing 8] It is the cross section of the semiconductor device by the gestalt 2 of operation of this invention.

[Drawing 9] It is a cross section for explaining the 1st process of the manufacturing process of the semiconductor device by the gestalt 2 of operation of this invention shown in drawing 8 .

[Drawing 10] It is a cross section for explaining the 2nd process of the manufacturing process of the semiconductor device by the gestalt 2 of operation of this invention shown in drawing 8 .

[Drawing 11] It is the cross section of the semiconductor device by the gestalt 3 of operation of this invention.

[Drawing 12] It is a cross section for explaining the 1st process of the manufacturing process of the semiconductor device by the gestalt 3 of operation of this invention shown in drawing 11 .

[Drawing 13] It is a cross section for explaining the 2nd process of the manufacturing process of the semiconductor device by the gestalt 3 of operation of this invention shown in drawing 11 .

[Drawing 14] It is a cross section for explaining the 3rd process of the manufacturing process of the semiconductor device by the gestalt 3 of operation of this invention shown in drawing 11 .

[Drawing 15] It is a cross section for explaining the 4th process of the manufacturing process of the semiconductor device by the gestalt 3 of operation of this invention shown in drawing 11 .

[Drawing 16] It is a cross section for explaining the 5th process of the manufacturing

process of the semiconductor device by the gestalt 3 of operation of this invention shown in drawing 11 .

[Drawing 17] It is the cross section having shown the modification of the semiconductor device by the gestalt 3 of operation of this invention.

[Drawing 18] It is the cross section of the semiconductor device by the gestalt 4 of operation of this invention.

[Drawing 19] It is a cross section for explaining the 1st process of the manufacturing process of the semiconductor device by the gestalt 4 of operation of this invention shown in drawing 18 .

[Drawing 20] It is a cross section for explaining the 2nd process of the manufacturing process of the semiconductor device by the gestalt 4 of operation of this invention shown in drawing 18 .

[Drawing 21] It is the cross section of the semiconductor device by the gestalt 5 of operation of this invention.

[Drawing 22] It is a cross section for explaining the 1st process of the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 23] It is a cross section for explaining the 2nd process of the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 24] It is the cross section having shown the 1st modification of the semiconductor device by the gestalt 5 of operation of this invention.

[Drawing 25] It is the cross section having shown the 2nd modification of the semiconductor device by the gestalt 5 of operation of this invention.

[Drawing 26] It is the cross section having shown the 3rd modification of the semiconductor device by the gestalt 5 of operation of this invention.

[Drawing 27] It is a cross section for explaining the 1st process of the 1st modification of the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 28] It is a cross section for explaining the 2nd process of the 1st modification of the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 29] It is a cross section for explaining the 3rd process of the 1st modification of the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 30] It is a cross section for explaining the 4th process of the 1st modification of

the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 31] It is a cross section for explaining the 5th process of the 1st modification of the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 32] It is a cross section for explaining the 1st process of the 2nd modification of the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 33] It is a cross section for explaining the 2nd process of the 2nd modification of the manufacturing process of the semiconductor device by the gestalt 5 of operation of this invention shown in drawing 21 .

[Drawing 34] It is the cross section of the semiconductor device by the gestalt 6 of operation of this invention.

[Drawing 35] It is a cross section for explaining the 1st process of the manufacturing process of the semiconductor device by the gestalt 6 of operation of this invention shown in drawing 34 .

[Drawing 36] It is the cross section of the semiconductor device by the gestalt 7 of operation of this invention.

[Drawing 37] It is a cross section for explaining the 1st process of the manufacturing process of the semiconductor device by the gestalt 7 of operation of this invention shown in drawing 36 .

[Drawing 38] It is a cross section for explaining the 2nd process of the manufacturing process of the semiconductor device by the gestalt 7 of operation of this invention shown in drawing 36 .

[Drawing 39] It is a cross section for explaining the 3rd process of the manufacturing process of the semiconductor device by the form 7 of operation of this invention shown in drawing 36 .

[Drawing 40] It is a cross section for explaining the 4th process of the manufacturing process of the semiconductor device by the form 7 of operation of this invention shown in drawing 36 .

[Drawing 41] It is the cross section having shown wiring by the DAMASHIN method of the conventional semiconductor device.

[Drawing 42] It is the cross section showing the semiconductor device which has the multilayer-interconnection structure by which the conventional proposal is made.

[Drawing 43] It is the cross section showing the semiconductor device which has the multilayer-interconnection structure formed by the conventional dual DAMASHIN

method.

[Drawing 44] It is the graph which showed the relation between the total capacity during wiring, and a design rule.

[Description of Notations]

1, 6, and 6a- 6c and 4 A layer insulation film, and 2, 2a and 2b Lower layer wiring 3, 3a-3t An etching stopper layer, 7a, 7b A slot, 11a-11e Resist pattern, 8 Conductor film, and 8a and 8b Wiring and 9 connection -- a hole and 10 Opening of an etching stopper layer, and 5, 5a-5d Covering film, and 12, 12a and 12b A barrier metal layer and 13 Opening.

[Abstract]

PROBLEM TO BE SOLVED: To provide a semiconductor device, with which the increase in the capacitances between wirings can be prevented and also the slow down of working speed can be prevented, and to provide a manufacturing method of the semiconductor device.

SOLUTION: This semiconductor device is provided with semiconductor regions 2a and 2b, a first insulating film 1, a coating film 3, a second insulating film 1, a coating film 3, the second insulating films 6a to 6c, and wiring layers 8a and 8b; and the first insulating film 1 is formed on the conductive regions 2a and 2b. The coating film 3 has a through-hole, with which the surface of the first insulating film 1 is exposed, and the coating film 3 is formed on the first insulating film 1. The second insulating films 6a to 6c are formed above the through-holes, and they have grooves 7a and 7b which are used to have the surface of the first insulating film 1 exposed. Wiring layers 8a and 8b are formed inside the grooves 7a and 7b.